

SEMICONDUCTOR PACKAGE

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

5 The present invention relates, in general, to semiconductor packages and, more particularly, but not by way of limitation, to a semiconductor package that can accommodate a larger semiconductor chip without increasing the foot print area afforded to a conventional semiconductor package. Additionally, the invention relates to a semiconductor package having an increased moisture path for increased overall package reliability.

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HISTORY OF RELATED ART

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It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal lead frames for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the lead frame are then incorporated. A hard plastic encapsulating material, or encapsulate, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

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As set forth above, the semiconductor package herein described incorporates a lead frame as the central supporting structure of such a package. A portion of the lead frame completely surrounded by the plastic encapsulate is internal to the package. Portions of the lead frame extend internally from the package and are then used to connect the package externally. More information relative to lead frame technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski, incorporated by reference herein. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at reduced costs, which results in increased consumer demand. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

A micro electronic circuit with a significant number of semiconductor chips are designed to conduct multiple functions in a minimal period of time. Additionally, semiconductor packages have become increasingly miniaturized with an increase in semiconductor package mounting density.

Demand for higher-speed, slimmer, and multi-functional electric appliances has lead to the development of semiconductor chips that have a high memory capacity without increasing thickness of the semiconductor chip. However, to achieve high memory capacity, the semiconductor chips must have an increased size. Therefore, to utilize slim semiconductor packages with multi-pins, there is a need for a technique of mounting the larger semiconductor packages.

A conventional small outline integrated circuit (SOIC) type semiconductor package is a surface-mounting type semiconductor package. Other types include a small outline J-bend (SOJ) type, a small outline package (SOP) type, and a quad flat package (QFP) type semiconductor package. Similar in structure to the SOIC type, these semiconductor packages differ from one to another only in the bend shape.

An SOIC type semiconductor package comprises a semiconductor chip, which has a plurality of bond pads on its upper surface along its circumference, and a chip paddle that is bonded to the bottom surface of the semiconductor chip via a conductive or non-conductive adhesive. A plurality of internal leads are arranged at regular intervals along the opposite sides of the semiconductor chip. External leads, which are bent in a seagull wing shape, are extended from the internal leads. Via conductive wires, such as gold or aluminum wires and bond pads of the semiconductor chip are electrically connected to the internal leads.

The semiconductor chip, the chip paddle, the conductive wires and the internal leads are encapsulated by an encapsulation material, to create a package body that has the function of preventing the internal components from being damaged by external factors, such as dust, heat, moisture, electrical and mechanical loads, etc. The encapsulation material can be thermoset plastics or thermoset resins, with the thermoset resins including silicones, phenolics, and epoxies.

Typically, the chip paddle, the internal leads and the external leads are made of copper (Cu) or alloy, collectively composing a leadframe.

While an area of the upper surface of the internal lead is plated with gold (Au) or silver (Ag) to improve the bonding strength with the conductive wires, an area of the external lead, which is to be fused onto a motherboard by soldering, is plated with nickel (Ni), tin (Sn) gold (Au), tin lead, nickel palladium, tin bismuth, or similar materials known in the art to minimize corrosion.

As described above, the conventional semiconductor package, in which the chip paddle occupies a larger space than does the semiconductor chip, has such a structure that results in difficulties with regard to securing a space for a large-size semiconductor chip. This is because the internal leads are spaced at regular intervals from each other and at a predetermined distance from the chip paddle.

Additionally, the internal leads formed in the semiconductor package are further extended over the package body from its front and rear sides or its front, rear, left and right sides. Thus, when such a semiconductor package is mounted on a motherboard, the semiconductor package occupies a significantly large space, which results in a decreased packaging density as well as adversely affecting design tolerance of electric patterns.

Further, when a large-size semiconductor chip is mounted in a semiconductor package of such a structure, the semiconductor package must be enlarged, which

decreases packaging density as well as increasing the size of the motherboard to accommodate the larger semiconductor chip. Thus, the motherboard's foot print area to which the external leads of the semiconductor package are fused must be re-designed.

5 A further drawback of conventional semiconductor chip design is that the semiconductor chip is completely encapsulated within a package body formed of a resinous material, which results in a very poor heat radiation ability.

SUMMARY OF THE INVENTION

10 The present invention relates to semiconductor packages that can accommodate a larger semiconductor chip. More particularly, one aspect of the present invention includes a semiconductor package comprising a semiconductor chip having a plurality of bond pads on its upper surface, a chip paddle bonded to the bottom surface of the semiconductor chip via an adhesive, and a plurality of internal leads, each having an etched part at the end facing the chip paddle. The internal leads are radially formed at regular intervals along the circumference of the chip paddle. Conductive wires electrically connect the bond pads of the semiconductor chip to the internal leads. A package body houses the semiconductor chip, the conductive wires, the chip paddle and the internal leads, which are encapsulated by an encapsulation material while the chip paddle and the internal leads are externally exposed at their side surfaces and bottom surfaces. In one version of the invention, a lower side area of the chip paddle is etched to the extent that the resulting etched part amounts to 10-90 % of the total area of the lower side area with preference to a location at the inside of the lower side area of the chip paddle. While the chip paddle and the lower surfaces of the internal leads are preferably in a common plane, the chip paddle may be thicker than the internal leads.

15 In another aspect, the semiconductor package of the present invention has a noticeable advantage over conventional SOIC type semiconductor packages, in that the semiconductor of the present invention can use a 3.5 folds larger semiconductor chip with the same volume as that of the conventional type semiconductor packages. In addition, in the semiconductor package of the present invention, the bottom surface of the internal lead, i.e., the position at which lands are formed, may be the same position at which the external leads are fused to the motherboard, so that a conventional foot print area can be utilized. Therefore, no design modification on the motherboard is required.

Moreover, the semiconductor package of the invention shows excellent heat radiation due to its bottom surface being exposed to the outside. Further, the etched part formed in the chip paddle brings about a remarkable improvement in the locking force between the chip paddle and the package body and in the fluidity of an encapsulation material during an encapsulation process. Additionally, the passage through which moisture permeates the semiconductor package is lengthened to minimize the influence of moisture on the semiconductor package. Typically, moisture permeates a semiconductor package at the interface between the encapsulate material and an exposed component, such as the chip paddle.

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BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

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Figure 1 shows a cross-sectional elevation view of a conventional semiconductor package;

Figure 2 is a top view of the conventional semiconductor package of Figure 1;

Figure 3 is a cross-sectional elevation view of a semiconductor package according to an embodiment of the present invention;

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Figure 4 is a perspective view of a semiconductor package according to an embodiment of the present invention wherein the semiconductor package is deprived of a package body;

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Figure 5 is a top view of a conventional semiconductor package of Figures 1 and 2 and the semiconductor package of Figure 3 showing that the two packages have the same foot print;

Figure 6 is a cross sectional view showing another embodiment of a semiconductor package according to the present invention;

Figure 7 is a cross sectional view showing another embodiment of a semiconductor package according to the present invention; and

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Figure 8 is a cross sectional view showing another embodiment of a semiconductor package according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention may be understood more readily by reference to the following detailed description of preferred embodiments of the invention and the figures.

Referring now to Figures 1 and 2, Figure 1 shows a cross sectional view of a conventional small outline integrated circuit (SOIC) type semiconductor package 10, which is a surface-mounting type semiconductor package. Figure 2 shows the conventional SOIC 10 in a top view. As shown, conventional SOIC type semiconductor package 10 comprises a semiconductor chip 12 that has a plurality of bond pads 14 on its upper surface along its circumference, and a chip paddle 16. Chip paddle 16 is preferably bonded to the bottom surface of the semiconductor chip 12 via a conductive or non-conductive adhesive. A plurality of internal leads 18, are arranged at regular intervals along opposite sides of the semiconductor chip 12. External leads 20, which are bent in a seagull wing shape, are extended from the internal leads 18. Conductive wires 22 are electrically connected to the internal leads 18. Conductive wires 22 are preferably made of gold or aluminum, although other materials may be used. The bond pads 14 of the semiconductor chip 12 are electrically connected to the internal leads 18.

The semiconductor chip 12, the chip paddle 16, the conductive wires 22 and the internal leads 18 are encapsulated by an encapsulation material, to create a package body 24, which has the function of preventing the internal constituents from being damaged by external factors, such as dust, heat, moisture, electrical and mechanical loads, etc. The encapsulation material may be thermoplastics or thermoset resins, with thermoset resins including silicones, phenolics, and epoxies.

Typically, the chip paddle 16, the internal leads 18 and the external leads 20 are made of copper (Cu), an alloy, or other conductive material. The chip paddle 16, the internal leads 18 and the external leads 20 collectively compose a leadframe.

An area of the upper surface of the internal lead 18 is preferably plated with gold (Au) or silver (Ag) to improve the bonding strength with the conductive wires 22. An area of the external lead 20, which is to be fused onto a motherboard by soldering, is plated with tin (Sn), gold (Au), tin lead, nickel palladium, tin bismuth, or any other similar material known in the art.

As described, conventional semiconductor package 10 has a chip paddle 16 that occupies a larger space than does the semiconductor chip 12. Therefore, conventional semiconductor package 10 has such a structure that it is not ideal for securing a large-size

semiconductor chip thereto since the internal leads 18 are spaced at regular intervals from one another and at a predetermined distance from the chip paddle 16.

In addition, the internal leads 18 that are formed in the conventional semiconductor package 10 are further extended over the package body 24 from its front and rear sides or its front, rear, left and right sides. Thus, when conventional semiconductor package 10 is mounted on a motherboard, the conventional semiconductor package 10 occupies a significantly large space, causing problems of decreasing packaging density on a motherboard, as well as problems related to design tolerance of electric patterns.

Further, when a large-size semiconductor chip is mounted in a conventional semiconductor package 10, the semiconductor package 10 must be enlarged, which causes a decrease in packaging density as well as an increase in the size of the motherboard. Thus, the foot print area of a motherboard to which the external leads 20 of the semiconductor package 10 are fused must be re-designed. Moreover, the semiconductor chip 12, which is thoroughly encapsulated within the package body 24 is very poor in heat radiation ability.

Referring now to Figures 3 and 4, Figure 3 shows a cross section of a semiconductor package 30 according to the present invention. Figure 4 shows a perspective view of the semiconductor package 30 deprived of a package body.

As shown in Figure 3, the semiconductor package 30 comprises a semiconductor chip 32 that has a plurality of bond pads 34 on its upper surface along its circumference, and a chip paddle 36, which is bonded to the bottom surface of the semiconductor chip 32 via a conductive or non-conductive adhesive 33.

Along the circumference of the chip paddle 36, a plurality of internal leads 38 are arranged at regular intervals. Internal leads 38 are as thick as the chip paddle 36 so that the upper surface of the internal lead 38 and the upper surface of the chip paddle 36 are in the same plane while the bottom surface of the internal lead 38 and the bottom surface of the chip paddle 36 are in the same plane. At an end facing the chip paddle 36, each of the internal leads 38 has an etched part 40 that is thinner than the internal lead 38 itself. Likewise, a lower side area of the chip paddle 36 is etched to the extent that the resulting etched part 42 amounts to 10-90 % of the total area of the chip paddle 36, which results in an improvement in the locking strength to the body 44 and the fluidity of an encapsulation material during the encapsulation step and minimizing the influence of

moisture on the semiconductor package 30. The influence of moisture is minimized by making lengthy the passage through which moisture permeates the semiconductor package 30. An electrical connection is formed between the bond pads 34 of the semiconductor chip 32 and the internal leads 38 through conductive wires 46. Conductive wires 46 are preferably made of gold wire or aluminum wire, although other materials may be used.

The semiconductor chip 32, the conductive wires 46, the chip paddle 36 and the internal leads 38 are encapsulated into a package body 44 wherein the bottom surface of the chip paddle 36 and the bottom surface of the internal lead 38 are in the same plane and are externally exposed in the downward direction of the package body 44. By being directly exposed to the outside of the package body 44, the semiconductor chip 32 exhibits improved heat radiation abilities as compared with conventional semiconductor chips, such as conventional semiconductor chip 10 (Figures 1 and 2). Typically, the chip paddle 36 and the internal leads 38 are made of copper (Cu) or alloy, although other materials may be used. The exposed portions of chip paddle 36 and internal lead 38 may, but do not have to be, coated or electroplated with a corrosion-minimizing material such as tin lead, tin, gold, nickel palladium, tin bismuth, or similar materials known in the art.

The sides of the internal leads 38 and the side of the body 44 form one plane, with the aim of securing a maximum volume in the body 44 to protect the semiconductor chip 32 and the conductive wires 46. Additionally, the inside surfaces of the internal leads 38 have etched parts 40 to improve the locking strength between the internal leads 38 and the package body 44.

Referring now to Figure 5, a top view of conventional semiconductor chip 10 is shown adjacent to a bottom view of a semiconductor package 30 of the invention. Reference lines 48 and 50 clearly indicate that conventional semiconductor package 10 and the semiconductor chip 32 of the invention have the same foot print. More particularly, it can be seen that external leads 20 of conventional semiconductor package 10 extend outwardly to reference line 48 above conventional semiconductor package 10 and to reference line 50 below conventional semiconductor package 10. Similarly, internal leads 38 of a semiconductor package 30 of the invention extend to reference line 48 above semiconductor package 30 and to reference line 50 below semiconductor package 30.

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Referring now to Figs. 6 through 8, shown are alternate embodiments of semiconductor packages of the invention. Because of similarities in many structural features to the semiconductor package 30 of a first embodiment, the semiconductor packages of Figures 6 through 8 will be described only for different structural features and similar features will retain the same numerical designations as the embodiment of Figure 3.

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Referring now to Fig. 6, semiconductor package 60 has a chip paddle 62, a lower side area of which is etched to the extent that the resulting etched part amounts to 10-90 % of the total area of the chip paddle 62. The etched part 64 provides the chip paddle 62 with additional areas that can be adhered to the package body 66 to improve the locking force between the chip paddle 62 and the package body 66. Additionally, the etched part 64 allows the encapsulating material to flow smoothly and has the effect of lengthening the passage through which moisture infiltrates the semiconductor package 60, so as to reduce problems attributed to moisture permeation on the semiconductor package, such as interfacial delamination and "popcorning" of the package when soldered to a circuit board.

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Referring now to Figure 7, shown is another alternate embodiment of a semiconductor package 70. Semiconductor package 70 has a chip paddle 72 with no etched parts on the lower surface of the chip paddle 72. Chip paddle 72 can easily radiate heat generated from the semiconductor chip 32 because of the enlarged exposed surface area on the lower surface of the chip paddle 72.

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Referring now to Figure 8, a further embodiment of a semiconductor package of the invention is designated generally 80. The chip paddle 82 is formed at a thickness different from that of the internal lead 38. The bottom surface of the chip paddle 82 and the bottom surface of the internal lead 38 are in a common plane. However, the upper surface of the chip paddle 82 is positioned at a higher level than is the upper surface of the internal leads 38. The chip paddle 82 is preferably 1.1-2.5 times as thick as the internal leads 38. Further, a lower side area of the chip paddle 82 is etched. The etched part 83 preferably has a thickness similar to that of the internal lead 38, so as to significantly improve the locking strength between the chip paddle 82 and the package body 84 as well as the fluidity of the encapsulation material upon the encapsulating. Preferably, the etched part 83 amounts to 10-90 % of the total area of the lower surface of the chip paddle 82.

5 Additionally, other embodiments are possible. For example, a semiconductor chip that is extended to the surface of the internal lead may be utilized. In this instance, the upper surface of the chip paddle forms a plane along with the upper surface of the internal leads. Alternatively, when the internal leads are positioned at a lower level than the semiconductor chip, the semiconductor chip can be mounted onto the chip paddle without the chip being limited to the size of the paddle. In such a case, a non-conductive adhesive tape is preferably used as the adhesive by which the semiconductor chip is bonded on the chip paddle or to the internal lead.

10 The invention has numerous advantages. Examples of advantages are set forth below, although other advantages are contemplated to fall within the scope of the invention and the below listed advantages are not intended to be limiting. One example of an advantage is that a semiconductor package according to the present invention can employ a semiconductor chip approximately 3.5 times as large as a conventional SOIC type semiconductor package having the same volume. A semiconductor chip package of the invention is able to accommodate a larger semiconductor chip while having the same footprint area afforded to a conventional semiconductor package.

15 Additionally, a semiconductor package according to the invention has improved locking strength between a chip paddle and an encapsulation material. Further, the present invention provides a semiconductor package that exhibits improved heat radiation of a semiconductor chip. In addition, in a semiconductor package of the present invention, the bottom surface of the internal lead, i.e., the position at which lands are formed, may have the same position at which the external leads are fused to the motherboard, so that a conventional foot print area can be utilized.

20 Moreover, the semiconductor package of the invention shows excellent heat radiation on account of its bottom surface being exposed to the exterior of the semiconductor package. Further, the etched part formed in the chip paddle brings about a remarkable improvement in the locking force between the chip paddle and the package body and in the fluidity of an encapsulation material during an encapsulation process. Additionally, the etched part makes lengthy the passage through which moisture permeates the semiconductor package to minimize the influence of moisture on the semiconductor package.

The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

| Attorney Docket No. | Title of Application | First Named Inventor |
|---------------------|---|----------------------|
| 45475-00015 | Semiconductor Package Having Increased Solder Joint Strength | Kil Chin Lee |
| 45475-00016 | Clamp and Heat Block Assembly for Wire Bonding a Semiconductor Package Assembly | Young Suk Chung |
| 45475-00018 | Near Chip Size Semiconductor Package | Sean Timothy Crowley |
| 45475-00020 | Stackable Semiconductor Package and Method for Manufacturing Same | Sean Timothy Crowley |
| 45475-00021 | Stackable Semiconductor Package and Method for Manufacturing Same | Jun Young Yang |
| 45475-00024 | Method of and Apparatus for Manufacturing Semiconductor Packages | Hyung Ju Lee |
| 45475-00028 | Semiconductor Package Having Improved Adhesiveness and Ground Bonding | Sung Sik Jang |
| 45475-00029 | Semiconductor Package Leadframe Assembly and Method of Manufacture | Young Suk Chung |

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It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. It will be obvious to a person of ordinary skill in the art that various changes and modifications may be made herein without departing from the spirit and the scope of the invention.